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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/781,784	02/20/2004	Shinichi Fujimoto	FJ-2003-055-US	6153

21254 7590 02/22/2008

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EXAMINER	
GILES, NICHOLAS G	

ART UNIT	PAPER NUMBER
2622	

MAIL DATE	DELIVERY MODE
02/22/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/781,784	FUJIMOTO, SHINICHI	
	Examiner	Art Unit	
	Nicholas G. Giles	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 December 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,5-7,17 and 18* is/are rejected.

7)☒ Claim(s) *3,4 and 8-16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 12/10/2007 have been fully considered but they are not persuasive.

Regarding claim 1, applicant argues that the frequency of the basic operating clock is not reduced at the time of AD conversion in Koide. The examiner notes that in 9:25-27 and 17:23-37 of Koide that the clock frequency is reduced for the TG 4 (timing generator) which in turn provides timing (clock) pulses to the A/D converter when the luminance is low. Therefore when the luminance is low the basic operating clock is reduced at the time of AD conversion.

Further regarding claim 1, applicant argues that frequency of the basic operating clock is not reduced at the time of AD conversion in Hasegawa. The examiner points out that in 7:30-44 of Hasegawa that the basic operating clock is always reduced at the time of AD conversion by the A/D drive 120.

2. Applicant's arguments, see page 9, filed 12/10/2007, with respect to claim 3 have been fully considered and are persuasive. The rejection of claim 3 has been withdrawn.

3. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a

reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

4. In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation to combine Smitt is that the RAM can be read out and used by the controller as Smitt discloses in 3:58-60.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim **18** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. Claim **18** recites the limitation "the clock change device" in line 5. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

8. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

9. Claims **1, 2, 6, 7, 17, and 18** are rejected under 35 U.S.C. 102(e) as being anticipated by Koide et al. (U.S. Patent No. 6,870,566).

Regarding claim **1**, Koide et al. discloses:

> An electronic camera in which an analog signal output from an image pickup device is AD-converted and digital processing is performed on the AD-converted signal on the basis of a basic operating clock (TG), said camera comprising: clock change device of changing the frequency of the basic operating clock (frequency divider 17:23-37); and control device of controlling the clock change device so that the frequency of the basic operating clock is reduced at the time of AD conversion of a still image output from the image pickup device (combination of system controller and image signal processor, 17:23-37 and Fig. 9).

Regarding claim **2**, see the rejection of claim 1 and note that Koide et al. further discloses:

> Photometry device of measuring the brightness of a subject (illuminance signal detector), wherein said control device controls the clock change device so that the frequency of the basic operating clock is reduced when it is determined that the brightness of the subject measured

by said photometry device is lower than a predetermined brightness (17:23-37 and Fig. 9).

Regarding claim **6**, see the rejection of claim 1 and note that Koide et al. further discloses:

Analog front end which receives said analog signal output from an image pickup device, and comprises an analog-to-digital converter which outputs said AD-converted signal (A/D 10 17:10-11).

Regarding claim **7**, see the rejection of claim 6 and note that Koide et al. further discloses:

A charge coupled device image sensor which supplies said analog signal to said analog front end (CCD 102, 3:38-42, 16:61-65, 17:4, 9:54-63, and Fig. 9); and a clock generation circuit which supplies an AD clock signal to said A/D converter and said image sensor (combination of timing generator 4, SSG 18, and frequency divider 17, 17:23-37).

Regarding claim **17**, Koide et al. discloses:

A signal processing circuit for an electronic camera including an image pickup device, said circuit comprising: a clock change device for changing a frequency of a basic operating clock (frequency divider 17:23-37); and a control device for controlling the clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device

(combination of system controller and image signal processor, 17:23-37 and Fig. 9).

Regarding claim **18**, Koide et al. discloses:

A method of processing an image data signal in an electronic camera including an image pickup device comprising: changing a frequency of a basic operating clock (frequency divider 17:23-37); and controlling a clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device (combination of system controller and image signal processor, 17:23-37 and Fig. 9).

10. Claims **1, 17, and 18** are rejected under 35 U.S.C. 102(b) as being anticipated by Hasegawa et al. (U.S. Patent No. 5,838,373).

Regarding claim **1**, Hasegawa et al. discloses:

An electronic camera in which an analog signal output from an image pickup device is AD-converted and digital processing is performed on the AD-converted signal on the basis of a basic operating clock, said camera comprising: clock change device of changing the frequency of the basic operating clock (A/D drive 122); and control device of controlling the clock change device so that the frequency of the basic operating clock is reduced at the time of AD conversion of a still image output from the

image pickup device (7:30-44 and Fig. 1, the clock is reduced for A/D conversion).

Regarding claim **17**, Hasegawa et al. discloses:

A signal processing circuit for an electronic camera including an image pickup device, said circuit comprising: a clock change device for changing a frequency of a basic operating clock (A/D drive 122); and a control device for controlling the clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device (7:30-44 and Fig. 1, the clock is reduced for A/D conversion).

Regarding claim **18**, Hasegawa et al. discloses:

A method of processing an image data signal in an electronic camera including an image pickup device comprising: changing a frequency of a basic operating clock (A/D drive 122); and controlling a clock change device such that the frequency of the basic operating clock is reduced at a time of AD conversion of a still image output from said image pickup device (7:30-44 and Fig. 1, the clock is reduced for A/D conversion).

Claim Rejections - 35 USC § 103

11. Claim **5** is rejected under 35 U.S.C. 103(a) as being unpatentable over Koide et al. in view of Smitt (U.S. Patent No. 5,502,578.

Regarding claim **5**, see the rejection of claim 1 and note that Koide et al. is silent with regards to an A/D converted signal being transferred from one line memory to RAM and then a second line memory to RAM of a still frame. Smitt discloses transferring one line of memory from the A/D converter to RAM of a still frame in 6:47-55, 3:21-57 and Fig. 2 where an eight bit word of RAM can be seen being transfer from the A/D converter to RAM. Transferring eight bits means there is a memory for storing a line of data. An advantage to doing this is that the RAM can be read out and used by the controller as Smitt discloses in 3:58-60. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to have Koide et al. include transferring one line of memory from the A/D converter to RAM of a still frame.

Koide and Smitt are silent with regards to using two line memories. Official Notice is taken that it was well known at the time the invention was made to using a pipelining architecture in image processing to include two line memories. An advantage to doing so is that, just like a pipeline, when one memory is being accessed for readout and processing by the processor, another line can be read into the other memory like a buffer so that the processor can immediately access the second memory when it is finished with the first instead of having to wait for the first memory to read another line. For this reason it would have been obvious to one of ordinary skill in the art at the time the invention was made to use two line memories.

It is noted by the examiner that because the applicant has failed to timely traverse the old and well-known statement above, it is now taken as admitted prior art. See MPEP 2144.03(c).

Allowable Subject Matter

12. Claims **3, 4, and 8-16** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding claim **3**, no prior art could be located that teaches or fairly suggests the frequency of the basic operating clock being reduced when a particular one of A plurality of modes is selected in combination with the rest of the limitations of the claim.

Regarding claim **4**, no prior art could be located that teaches or fairly suggests changing the basic operating clock frequency to be lower based on the ISO speed in combination with the rest of the limitations of the claim.

Regarding claim **8**, no prior art could be located that teaches or fairly suggests an amplifier controlling a gain of a signal output from the CDS and the A/D converter receiving the gain controller signal in combination with the rest of the limitations of the claim.

Regarding claims **9-15**, these claims depend on claim 8 and therefore are objected to.

Regarding claim **16**, no prior art could be located that teaches or fairly suggests not reducing the frequency of the basic operating clock at a time other than time of AD conversion in combination with the rest of the limitations of the claim.

Conclusion

13. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nicholas G. Giles whose telephone number is (571) 272-2824. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

NGG

LIN YE
SUPERVISORY PATENT EXAMINER